The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MARCO RACANELLI

Appeal No. 2006-2832
Application No. 09/833,953

ON BRIEF

Before HAIRSTON, MACDONALD and LUCAS, Administrative Patent Judges.

LUCAS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1, 3 to 12, 14, 15, and 17 to 23. Claims 2, 13 and 16 have been canceled.

Invention

Appellant describes his invention as follows:

According to the invention, a layer is formed over a transistor gate and a field oxide region. For example, a polycrystalline silicon layer can be deposited over a PFET gate oxide and a silicon dioxide isolation region on the same chip. The layer is then doped over the transistor gate without doping the layer over the field oxide. A photoresist layer can be used as a barrier to implant doping, for example, to block N+ doping over the field oxide region. The entire layer is then doped, for example, with P type dopant after removal of the doping barrier. The second doping results in formation of a high resistivity resistor over the field oxide region, without affecting the transistor gate. Contact regions are then formed of an appropriate material, for example a silicide, for connecting the resistor to other devices.

Claims 1 and 14 are representative of the claimed invention and are reproduced as follows:

1. A method comprising steps of:

forming a layer over a transistor gate region and a field oxide region, said transistor gate region being situated over a well and said field oxide region not being situated over said well, wherein said field oxide region and said well are situated in a substrate;

forming a doping barrier above said layer over said field oxide region after said step of forming said layer;

doping said layer over said transistor gate region with a first dose of a first dopant after said step of forming said doping barrier, wherein said dose of said first dopant is a dosage greater than required to result in said layer over said transistor gate region having transistor gate electrical properties, wherein said first dopant has a first conductivity type;

removing said doping barrier after said step of doping said layer over said transistor gate region with said first dose of said first dopant;

doping said layer over said transistor gate region and said field oxide region with a second dose of a second dopant so as to form a high resistivity resistor in said layer over said field oxide region after said step of removing said doping barrier, wherein said second dopant has a second conductivity type, wherein said first dose of said first dopant is higher than said second dose of said second dopant such that said transistor gate electrical properties are unaffected by said second dose of said second dopant;

forming a silicide blocking oxide layer over an inner portion of said layer over said field oxide region after said step of doping said layer over said transistor gate region and said field oxide region with said second dose of said second dopant;

doping an outer portion of said layer over said field oxide region with a third dopant so as to form a high-doped region in said outer portion of said layer over said field oxide region after said step of forming said silicide blocking oxide layer over said inner portion of said layer over said field oxide region, wherein said third dopant has said second conductivity type;

fabricating a contact region for said high resistivity resistor over said high-doped region in said outer portion of said layer over said field oxide region after said step of doping an outer portion of said layer over said field oxide region, wherein said contact region comprises a silicide.

14. A method comprising steps of:

depositing a polycrystalline silicon layer on a chip, said polycrystalline silicon layer including a gate region and a resistor region, said gate region being situated over a well and said resistor region not being situated over said well, wherein said field oxide region and said well are situated in a substrate;

forming a doping barrier above said polycrystalline silicon layer after said step of depositing said polycrystalline silicon layer so as to prevent doping of said resistor region of said polycrystalline silicon layer;

doping said polycrystalline silicon layer with a first dose of a first dopant after said step of forming said doping barrier, wherein said dose of said first dopant is a dosage greater than required to result in said layer over said gate region having transistor gate electrical properties, wherein said first dopant has a first conductivity type;

removing said doping barrier after said step of doping said polycrystalline silicon layer with said first dose of said first dopant;

doping said polycrystalline silicon layer with a second dose of a second dopant after said step of removing said doping barrier so as to form a high resistivity resistor in said resistor region of said polycrystalline silicon, wherein said second dopant has a second conductivity type, wherein said first dose of said first dopant is higher than said second dose of said second dopant such that said transistor gate electrical properties are unaffected by said second dose of said second dopant;

forming a silicide blocking oxide layer over an inner portion of said polycrystalline silicon layer over said field oxide region after said step of doping said polycrystalline silicon layer with said second dose of said second dopant;

doping an outer portion of said resistor region of said polycrystalline silicon layer with a third dopant after said step of forming said silicide blocking oxide layer

so as to form a high-doped region in said outer portion of said resistor region, wherein said third dopant has said second conductivity type;

fabricating a contact region over said high-doped region in said outer portion of said resistor region of said polycrystalline silicon layer after said step of doping said outer portion of said resistor region of said polycrystalline silicon layer, said contact region being electrically connected to said resistor region, wherein said contact region comprises a silicide.

References

The references relied on by the Examiner are as follows:

Zaccherini	5,436,177	Jul. 25, 1995
Erdeljac et al. (Erdeljac)	5,489,547	Feb. 6, 1996
Shao et al. (Shao)	6,156,602	Dec. 5, 2000

Rejections At Issue

Claims 1, 3 to 12, 14, 15, and 17 to 23 stand rejected under 35 U.S.C. § 103 as being obvious over Zaccherini in view of Erdeljac and Shao.

Throughout our opinion, we make references to the Appellant's briefs, and to the Examiner's Answer for the respective details thereof.[1]

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1 Appellant filed an appeal brief on February 13, 2006. Appellant filed a reply brief on June 13, 2006. The Examiner mailed an Examiner's Answer on April 11, 2006.

Opinion

With full consideration being given to the subject matter on appeal, the Examiner's rejections and the arguments of the Appellant and the Examiner, for the reasons stated infra, we reverse the Examiner's rejection of claims 1 and 3 to 12 under 35 U.S.C. § 103(a), and we sustain the Examiner's rejection of claims 14, 15, 17 to 23 under the same statute.

Whether the Rejection of Claims 1, 3 to 12, 14, 15, and 17 to 23 Under 35 U.S.C. § 103(a) is proper?

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the invention as set forth in claims 1 and 3 to 12. Accordingly, we reverse.

Consider claim 1 as exemplary of this group of claims. Arguments over limitations in the dependent claims have not been presented, and will not be discussed.

In this analysis, we will review first the elements of the claim, and then the arguments concerning motivation to combine the teachings of the references.

Elements of the Claim: Claims 1 and 3 to 12

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a *prima facie* case of obviousness. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). See also In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984).

The examiner presents three references, Zaccherini, Erdeljac and Shao, to demonstrate the elements of the prior art relevant to the rejection of these claims. All three references present methods for producing semiconductor electronic devices with doped polycrystalline layers formed on a substrate and concurrently producing one or more field effect transistors (FETs) and one or more resistors.

Specifically, and in reference to claim 1, Zaccherini forms a layer (7) over a transistor gate region (4) and a field oxide region (5). Erdeljac shows elements of the claimed well, which we discuss in more detail below. Zaccherini forms a doping barrier (10) above the layer, and applies a first dose of a first dopant (11) of a first conductivity type at a dosage greater than that required for forming the

transistor gate region electrical properties (4), removes said doping barrier (10) and dopes said layer over said transistor gate region (4) and said field oxide region (5) with a second dose of a second dopant (13) of a second conductivity type, where the first dose is higher than said second dose, and where the electrical properties of the transistor gate are unaffected by said second dose. The ranges will be discussed below. The reference Shao teaches forming a silicide blocking oxide layer (Shao – 60) over a portion of said layer over the field oxide region (Shao – 12), doping with an additional dose of the dopant of the second conductivity type, and fabricating contact regions (Shao – column 8, lines 9 ff).

Appellant presents a number of arguments against this *prima facie* case for obviousness. His first argument is to indicate that each of the references lacks one or more features of the claims, notwithstanding the examiner's assertions that those missing elements are in another of the references. For example, at the bottom of page 7 of the Brief, Appellant remarks, "However, Zaccherini fails to teach, disclose, or suggest forming a layer over a transistor gate region, which is situated over a well in a substrate." It is noted that the Examiner has presented such wells to be in the prior art by referring to the teachings of Erdeljac. One cannot show

nonobviousness by attacking references individually where the rejections are based on combinations of references. See In re Keller, 642 F.2d 413, 426, 208 USPQ 871, 882 (CCPA 1981); In re Merck & Co., 800 F.2d 1091, 1097, 231 USPQ 375, 380 (Fed. Cir. 1986).

Appellant then argues that "Thus, in Zaccherini, the respective implant dosage ranges of the N type dopant and the P type dopant overlap" (Brief, page 8). Zaccherini indicates a preferred range for the N type dopant between 1 x 10^{15} and 1 x 10^{16} ions/cm^2 (column 3, line 28) and a range for the P type second dopant between 1 x 10^{12} and 1 x 10^{15} ions/cm^2 (column 3, line 51). Although the first range is "contemplated" by Zaccherini at broader figures mentioned by Appellant (5 x 10^{14} to 1 x 10^{16}), the surrounding text clearly indicates that the first dose is intended to be heavy, and the second dosage is intended to be medium or low (column 3, line 49). We find that the teaching is a first range higher than the second, as claimed, and not overlapping as argued.

However, Appellant further argues that "Erdeljac fails to teach, disclose, or remotely suggest a transistor gate region situated over a well and a field oxide

region not situated over the well..." (Brief, page 10). Examiner notes "It would have been within the scope of one of ordinary skill in the art to combine the teachings so Zaccherini and Erdeljac et al. to enable forming the gate transistors and field oxide regions of Zaccherini on the substrate of Erdeljac et al...." (Examiner's Answer, page 4). Looking closely at Erdeljac, Figure 11, we observe that field oxide region 20 clearly extends through the transistor gate region over the N well and under the resistors. The teaching of the claimed limitation "said field oxide region not being situated over said well" is not within the teaching of Erdeljac, Zaccherini or Shao.

The rejection of claims 1, 3 to 12 under 35 U.S.C. § 103(a) is thus reversed.

Elements of the Claim: Claims 14, 15 and 17 to 23

Claim 14 is exemplary of this group of claims, recited *supra*. Though Appellant indicates that claim 14 recites "similar limitations as independent claim 1" discussed above (Brief, page 16), the claim is distinguishable from claim 1 for reciting "depositing a polycrystalline silicon layer on a chip, said polycrystalline silicon layer including a gate region and a resistor region, said gate region being

situated over a well and said resistor region not being situated over said well, wherein said field oxide region and said well are situated in a substrate...."

Continuing the analysis used with claim 1 above, applied now to claim 14, we note in Erdeljac, in Figure 11, a resistor region containing resistors 32, 34, 56 and transistor gate region 24 over N well 18, with the resistor region not being situated over said well. Thus, we find a teaching in Erdeljac of the claimed subject matter of claim 14.

Appellant has not separately argued the contents of the claims dependent on claim 14, and we concur with the Examiner that their limitations are obvious over the prior art as demonstrated by the references Zaccherini in view of Erdeljac and Shao.

Motivation to Combine

Appellant argues that the motivation to combine these references is impermissible hindsight. For guidance on this issue, we consider the following:

> While this court indeed warns against employing hindsight, its counsel is just that – a warning. That warning does not provide a rule of law that an express, written motivation to combine must appear in prior art references before a finding of obviousness. Stated differently, this court has consistently stated that a court or examiner may find a motivation to combine prior art references in the nature of the problem to be solved. Ruiz v. A.B. Chance Co., 357 F.3d 1270, 1276, 69

USPQ2d 1686, 1690 (Fed. Cir. 2004); Also Pro-Mold & Tool Co. v. Great Lake Plastic Inc., 75 F.3d 1568, 1573, 37 USPQ2d 1626, 1630; In re Huang, 100 F.3d 135, 139 n.5, 40 USPQ2d 1685, 1688 n.5 (Fed. Cir. 1996).

The claimed invention relates to the "fabrication of CMOS... semiconductor devices." An objective of the application is to "simplify the fabrication process whenever possible by, for example, eliminating steps or finding compatible processes" (Specification, page 3). Thus, the claimed invention addresses forming a field effect transistor (FET) on a silicon wafer concurrently with the formation of resistors used in the circuitry with that transistor. The cited reference Zaccherini teaches a method for forming a FET on a layer of polycrystalline silicon (region 4) along with resistors (8) formed with the same layer in a method hauntingly similar to the claimed method. Erdeljac teaches forming a FET (50) and a few resistors (20, 32 and 34) on a common silicon wafer in which a N-well is employed, and Shao teaches forming a FET (40) and resistor (38) and employing a blocking layer for the resistor. All references express an objective of simplifying the process and reducing costs.

In the recent case In re Kahn, 441 F.3d 977, 985, 78 USPQ2d 1329, 1335 (Fed. Cir. 2006), the Board was guided:

> "... to establish a *prima facie* case of obviousness based on a combination of elements disclosed in the prior art, the Board must articulate the basis on which it concludes that it would have been obvious to make the claimed invention. *Id.* [*Graham v. John Deere Co.*, 383 U.S. 1, 13-14 [148 USPQ 459] (1966)] In practice, this requires that the Board "explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious." *Id.* at 1357-59.

With the teachings of Zaccherini, Erdeljac and Shao before us, all of whom present building a combination of transistor(s) and resistor(s) on a silicon substrate using various combinations of the same fabrication steps, we conclude that one of ordinary skill in this art would be motivated to minimize the number of layers and thus costs, and thereby would be motivated to incorporate the teachings of the N-well of Erdeljac and the blocking layer of Shao in the process of Zaccherini.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would have suggested to one of ordinary skill in the art the invention as set forth in claims 14, 15 and 17 to 23.

CONCLUSION

In view of the forgoing discussion, the rejection of claims 1 and 3 to 12 is reversed. The rejection of claims 14, 15 and 17 to 23 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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